



# DAT Call for Papers

April 21-24, 2025  
Hsinchu, Taiwan

The 2025 International VLSI Symposium on Technology, Systems and Applications (VLSI TSA) will be held on April 21-24, 2025 at the Ambassador Hotel Hsinchu, Taiwan. Original and unpublished papers on all aspects are solicited, including but not limited to the following scope.

## SCOPE

### ANALOG, MIXED-SIGNAL, and RF DESIGN

- Analog and Mixed-Signal Circuits
- Data Converters
- Power Management Circuits
- Wireless Transmitter and Receiver Circuits
- Wired System and IO Design
- Sensor and Interface Circuits

### DIGITAL, MEMORY, and AI CHIP DESIGN

- Asynchronous and Neuromorphic Computing Circuits
- Communication Baseband Designs
- Computing-in-Memory
- Digital AI Chips
- Digital Circuits and ASICs
- Hardware Security and Trust Circuits for IoT and AI
- Low Voltage & Ultra Low-Power Circuits and Systems
- Memory Circuits and Systems

### APPLICATION, SOFTWARE and HARDWARE, and AI SYSTEM

- AI for Systems and Systems for AI
- CPU, DSP, and Multicore Architectures
- Domain-Specific Architectures and Accelerators
- Embedded System and Software
- Hardware-efficient AI Methods
- Multimedia Processing Designs
- SoC (System on Chip) and NoC (Network on Chip)
- Software/Hardware Co-Design and System Compiler
- SiP (System-in-Package) and Heterogeneous Integration

### DESIGN AUTOMATION and TEST METHODOLOGY

- AI for Design Automation & Test
- Behavioral, Logic, and Physical Synthesis
- Design Automation & Test for Analog/Mixed-Signal/RF, 2D/3D IC, Memory, Biochip, AI Chips, and Emerging Systems
- Design for Manufacturability, Testability, and BIST
- Design Verification, Modeling, and Simulation
- Power/Thermal/Timing Optimization and On-Chip Monitoring
- Silicon Debug, Diagnosis, ECO, and Yield/Reliability Enhancement
- Test Generation, Compression, and Test Standards

### EMERGING TECHNOLOGY

- Circuit & IP Design Based on New Transistor Technology, e.g., Fork-Fin FET, Sheet FET, GAA FET, and C-FET
- Cryogenic Circuits and Systems
- Flexible and Printable Electronics
- Medical/Bio-electronics/Bio-inspired Chip Designs
- Quantum Computing
- Silicon Photonics

## GENERAL INSTRUCTIONS

- Prospective authors must electronically submit the self-contained paper with figures and tables via the conference submission page (<https://expo.itri.org.tw/2025DAT/Submission>) before December 2, 2024 (23:59 GMT+8).
- The submitted manuscript must be 2 or 4 pages including references, double-columned, IEEE-style compatible, in PDF format only. Any submissions not adhering to the rules will be rejected immediately without review.
- Before submitting your abstract/paper, please review the information on IEEE Intellectual Property Rights at <https://www.ieee.org/publications/rights/index.html>
- The review process will be double-blind.
  - Please do **NOT** reveal any authors' information (names, affiliations, email, grant information, personal acknowledgment, etc.) anywhere in the initial manuscript. You must also ensure that the metadata in the PDF does not include such information.
  - All references, including authors' previous work, should be referred as 3rd-persons' works. E.g., you should use "This paper presents a new method to improve XXX's approach [1]." instead of "This paper presents a new method to improve our previous approach [1]." Do NOT omit or anonymize references for blind review.
  - The initial manuscript violating the double-blind review policy will be rejected.
- Accepted papers **MUST** be presented **in person** by one of the authors at the symposium, and the presentation must be conducted in English. All accepted manuscripts in the proceeding will be published in IEEE Xplore.
- Any changes on the title or author list or withdrawal after acceptance must be approved by DAT Program Chairs.
- All paper presenters are required to register for the symposium.
- No-show papers will not be included in the symposium proceedings and will not be submitted to the IEEE Xplore database.
- Please refer to the detailed information on the conference website for authors: <https://expo.itri.org.tw/2025VLSITSA>

## STUDENT SUBSIDY

- Student Travel Financial support for attending 2025 VLSI TSA is available for full-time student presenters living outside of Taiwan.

## BEST PAPER AWARD

Three best papers will be selected this year through a rigorous evaluation process conducted by the DAT technical program committee and session chairs.

## IMPORTANT DATES (Note: All are based on Taiwan time, which is eight hours ahead of Greenwich Mean Time (GMT+8).)

Paper Submission Deadline	December 2, 2024
Notification of Acceptance	January 24, 2025
Deadline for Final Paper (IEEE compatible version) Submission	February 28, 2025
Deadline for Author Registration	February 28, 2025

## DAT PROGRAM CHAIRS:

Kenichi Okada, Tokyo Institute of Technology

Tai-Cheng Lee, National Taiwan University

Ming-Der Shieh, Industrial Technology Research Institute